REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 7, 19, and 22 have been amended. Claims 24-31 are allowed. Claims 7-13 and 19-33 are pending.

35 U.S.C. §102

Claims 7, 9-13 and 32 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,200,862 to Gardner et al. (hereinafter, "Gardner"). Applicant respectfully traverses the rejection.

Claim 7 has been amended and, as amended, recites a method [portions of the amended language appear in bold italics below] comprising:

- depositing a layer of oxide proximate a first surface of a semiconductor substrate;
- forming a gate oxide layer on the first surface, adjacent to the deposited oxide layer;
- ***after the depositing of the layer of oxide,*** forming a pair of active areas in the first surface, adjacent the deposited oxide layer and gate oxide layer;
- forming a gate electrode by depositing a conductive layer over the gate oxide layer;
- depositing a dielectric layer over the gate electrode, active areas, and deposited oxide layer; and
- forming electrical contacts to the pair of active areas and the gate electrode.

Support for this amendment can be found throughout the application as originally filed. Gardner does not disclose these aspects.

Gardner is directed to a mask for asymmetrical transistor formation with paired transistors. Gardner discloses the first step for producing the transistor as follows:

> Substrate 10 has already had formed therein, e.g., by ion implantation, a channel region 14, a punch-through region, and a well region. (Only the channel region 14 is illustrated.) The substrate can be doped with arsenic or phosphorous ions to form an n-doped channel regions (or

> n-channel regions). The substrate can be doped with boron ions to form a p-doped channel (or p-channel) regions. *Gardner, Col. 3, Lines 24-31.*

Gardner then discloses that "[a]fter formation of doped regions in the substrate 10, a gate dielectric layer 22, of 10-30 ANG. is formed by oxide growth, plasma deposition, or low pressure chemical vapor deposition." *Gardner, Col 3, Lines 52-55.* After which, Gardner discloses a patterning of layer 30 for ion bombardment to form a resulting device having asymmetric source/drain regions. *See Gardner, Col. 4, Lines 14-36.* Finally, Gardner discloses formation of a dielectric layer as follows:

> The photoresist regions 30 are removed and a dielectric layer 40, typically silicon oxide is formed and planarized. Vias are formed in the dielectric layer 40 exposing the surfaces of the substrate source/drain regions 28[1], 34 and the surfaces of the gate electrode of gate structure 20. *Gardner, Col 4, Lines 40-44.*

Thus, Gardner discloses the formation of the dielectric layer 40 after the formation of the source/drain regions.

Nowhere in Gardner is there discussion, teaching or suggestion for depositing a layer of oxide proximate a first surface of a semiconductor substrate and ***after the depositing of the layer of oxide,*** forming a pair of active areas in the first surface, adjacent the deposited oxide layer and gate oxide layer as recited in claim 7. This statement is also supported by the Office Action. For example, as correctly stated by the Office Action at page seven of the *Office Action Dated March 31, 2004,* "Gardner et al. teach forming the deposited oxide layer 40 *after* forming the active areas 28/24". For at least these reasons, claim 7 is allowable over Gardner. Applicant respectfully requests that the §102 rejection of claim 7 be withdrawn.

Claims 8-13, and 32 depend from claim 7 and are allowable for at least the same reasons as stated with respect to claim 7. Therefore, Applicant

respectfully requests that the §102 rejection of claims 9-13, and 32 be withdrawn, and the §103 rejection of claim 8 be withdrawn.

35 U.S.C. §103

Claims 22-23 are rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,635,968 to Bhaskar et al. (hereinafter, "Bhaskar") in view of U.S. Published Application No. 2002/0058368 to Tseng (hereinafter, "Tseng"). Applicant respectfully traverses the rejection.

Claim 22 has been amended and, as amended, recites a method [portions of the amended language appear in bold italics below] comprising:

- depositing a layer of oxide proximate a first surface of a semiconductor substrate;
- exposing a portion of the first surface of the semiconductor substrate; and
- forming a field effect transistor (FET) on the exposed portion of the first surface of the substrate having the deposited oxide layer, wherein the FET includes a gate electrode with associated active areas formed after the exposing the first surface of the semiconductor substrate, ***and is electrically isolated by the deposited layer of oxide***.

Support for this amendment can be found throughout the application as originally filed. Neither Bhaskar nor Tseng, alone or in combination, disclose or suggest these aspects.

The Office Action asserts Bhaskar for teaching a method of forming a semiconductor device. The Office Action then asserts Tseng for "forming a deposited oxide 48 on the substrate 42 (Fig. 2A); exposing a first surface (i.e. top surface) of the substrate 42 via a formation of a trench 51 (Fig. 2B); and forming active area 52 (i.e. impurity region by ion implanting through the trench 51 after exposing the first surface (Fig. 2B)." *Office Action Dated*

March 31, 2004, Page 5. Tseng, however, describes removal of the sacrificial layer 48, as shown in the following excerpts:

> First, a sacrificial layer 48 and a first photoresist layer 50 are sequentially formed on the substrate 42. The sacrificial layer 48 is formed by depositing a pad oxide layer and a silicon nitride layer on the substrate 42. The photoresist layer 50 is patterned to expose a first predetermined area of the sacrificial layer 48 on region B. As shown in FIG. 2B, by using the first photoresist layer 50 as a mask, a first trench 51 is formed in the sacrificial layer 48 to expose the substrate 42, and then the first photoresist layer 50 is stripped off. Next, using the sacrificial layer 48 as a mask, n-type impurity ions are implanted into the exposed substrate 12 to form a first impurity layer 52. *Tseng, Paragraph 20, Lines 10-21.*
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> As shown in FIG. 2E, a gate insulating layer 56 is formed on the bottom of the first trench 51, the second trench 53, and the third trench 53, and a polysilicon layer 58 is then deposited on the substrate 42 to fill the first trench 51, the second trench 53, and the third trench 53. Next, by using a mask, the polysilicon layer 58 and ***the sacrificial layer 48 outside the trenches 51, 53, 55 are removed.*** As a result, as shown in FIG. 2F, the polysilicon layer 58 remaining in the second trench 53 on region A serves as a gate electrode 58a of the internal circuit device, the polysilicon layer 58 remaining in the third trench 55 on region B serves as a gate electrode 58b of the ESD protecting device, and the polysilicon layer 58 remaining in the first trench 51 over the first impurity layer 52 on region B serves as a dummy gate electrode 58c of the internal circuit device. *Tseng, Paragraph 22 (emphasis added).*

Thus, Tseng describes that "by using a mask, the polysilicon layer and the sacrificial layer 48 outside the trenches 15, 53, 55 are removed." *Tseng, Paragraph 22, Lines 5-6.* Because Tseng describes the removal of the sacrificial layer 48, as a consequence, the sacrificial layer 48 is not included in the FET described by Tseng and the sacrificial layer 48 does not electrically isolate the associated active areas of the FET. Nowhere in Bhaskar nor Tseng,

alone or in combination, is there discussion, teaching or suggestion for the depositing, exposing and forming as claimed in claim 22. Accordingly, for at least this reason, claim 22 is allowable over Bhaskar and Tseng.

Claim 23 depends from claim 22 and is allowable for at least the same reasons as stated with respect to claim 22. Therefore, Applicant respectfully requests that the §103 rejection of claim 23 be withdrawn.

35 U.S.C. §103

Claims 19-21 and 33 are rejected under 35 U.S.C. §103 as being unpatentable over Bhaskar in view of U.S. Patent No. 6,318,846 to Saul et al. (hereinafter, "Saul"). Applicant respectfully traverses the rejection.

Claim 19 has been amended and, as amended, recites a method [portions of the amended language appear in bold italics below] comprising:

- manufacturing a fluid ejection device by:
  - depositing a current prevention layer proximate a first surface of a semiconductor substrate; and
  - forming first and second field effect transistors (FETs), wherein each said FET includes a gate electrode with associated active areas formed in the first surface of the semiconductor substrate having the current prevention layer ***thereon***, wherein the current prevention layer includes a region that minimizes current flow between the active areas of the first FET with respect to the active areas of the second FET.

Support for this amendment can be found throughout the application as originally filed. Neither Bhaskar nor Saul, nor any of the other submitted references, alone or in combination, disclose or suggest the method of manufacturing a fluid ejection device as claimed.

The Office Action asserts Bhaskar for manufacturing a semiconductor device and then Saul for forming a plurality of FETs. However, as correctly asserted by the Office Action in relation to Claim 22, "Bhaskar et al. are silent as to the associated active areas 907 and 911 are formed after the exposing in

the first surface of the semiconductor substrate 901". *Office Action dated March 31, 2004, Page 4.* Therefore, Bhaskar does not disclose, teach or suggest a FET that includes a gate electrode with associated active areas formed in the first surface of the semiconductor substrate having the current prevention layer thereon as claimed in Claim 19. Saul does not cure the defects of Bhaskar. Accordingly, for at least this reason, this claim is allowable.

Claims 20-21 and 33 depend directly from claim 19 and are allowable for at least the same reasons as stated with respect to claim 19. These claims are also allowable for their own recited features which, in combination with those recited in claim 19, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Allowable Subject Matter

The Office Action indicated that Claims 24-31 are allowed.

Conclusion

All pending claims 7-13 and 19-33 are in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully submitted,

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